SEMINAR

MECHANICS and MATERIALS CHALLENGES IN ELECTRONIC PACKAGING

ABSTRACT

Electronic packaging has typically been defined as providing an enabling function and a space transformer between the IC feature sizes and the board & system level interconnects and has grown to become a ubiquitous part of the overall electronic assembly. However, in certain market segments, such as flash memories, the package has evolved to become a key product differentiator and performance enabler. The scope of electronic packaging is very broad across multiple application areas such as CPU’s and Chipsets for the desktop, mobile and server segments, hand-held and wireless devices, telecom components & network processors, and memory devices; with each segment potentially having its unique set of demands and constraints such as the form factor, function, cost, reliability requirements, thermal and electrical performance.

To ensure that right technical and cost-effective solutions are defined, developed and deployed across the different market segments, electronic packaging provides significant research and development challenges and opportunities across multiple disciplines including materials, mechanics, reliability, thermals, high speed interconnects, power delivery and manufacturing.

This presentation will first provide an overview of current and future package technologies and associated demands in the different market segments, followed by a focus on current metrology challenges in the areas of mechanical model validation and material strength and property characterization.

MICHAEL MELLO

Michael Mello has been a Senior Packaging Engineer at Intel Corporation since 1997. Mike is a member of the Mechanical Core Competency group within the Assembly Test & Development Organization located in Chandler Arizona. He is responsible for managing the Experimental Mechanics lab at the Intel ATD Chandler site and oversees the proliferation of tools and measurement techniques to Intel labs worldwide.

Mr. Mello received a BS degree in Physics from the Massachusetts State College System in 1985 and an MS degree in Optical Engineering from the University of Rochester - Institute of Optics, in 1988. Prior to his tenure at Intel, Mike was a Senior Research Engineer at the Brown University Division of Engineering from 1988 – 1997 where he worked with Dr. Rodney J. Clifton on high strain rate testing methods and the development of interferometry techniques with application to plate impact testing.

Mr. Mello has authored several papers on interferometry techniques in the field of Applied Mechanics and was awarded an outstanding paper award at the 2003 ECTC for a paper titled “Laser Spallation Adhesion Metrology for Electronic Packaging Development”. He can be reached by email at michael.mello@intel.com

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Sumwalt Room 102

DATE: Thursday, August 18, 2005

TIME: 4:00 PM to 5:00 PM

Light refreshments will be served