Development of DSP-based Electromechanical (E/M) Impedance Analyzer for Active Structural Health Monitoring

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ABSTRACT

The electromechanical (E/M) impedance method is a powerful technique in active structural health monitoring (SHM). E/M impedance method utilizes as its main apparatus an impedance analyzer that reads the in-situ E/M impedance of piezoelectric wafer active sensors (PWAS) attached to the monitored structure. Present-day impedance analyzer equipments (e.g. HP4194) are bulky, heavy and expensive laboratory equipment that cannot be carried into the field for on-site structural health monitoring.

This paper presented the development of a compact and low-cost impedance analyzer system. First, two types of impedance measurement approaches were evaluated in a PC-based simplified impedance analyzer system. It was found that the first approach, which measures impedance frequency by frequency, is very accurate but is not time-efficient and needs more efforts to be implemented. As for the second approach, which measures impedance using broad-band excitation and transfer function method, provides a good compromise among the measurement time-efficient, accuracy and implementation efforts. Experimental results show that this approach can be used for E/M impedance method for structural health monitoring. Second, to eliminate the PC in the measurement system, a DSP-based impedance analyzer system is proposed for further miniaturization. The system hardware configuration and design, software state flow for impedance measurement, and preliminary testing were presented in details.

Keyword: piezoelectric wafer active sensors, structural health monitoring, DSP, impedance analyzer, impedance measurement, PWAS

1. INTRODUCTION

The electromechanical (E/M) impedance method is a new embedded ultrasonics method that is emerging as an effective and powerful technique for structural health monitoring [1]. Using PWAS (piezoelectric wafer active sensor) permanently attached to the structure, the E/M impedance method directly measures the high-frequency local impedance spectrum of the structure. Since high-frequency local impedance spectrum is much more sensitive to incipient damage than low-frequency global impedance, the E/M impedance method is considered to be better suited for applications in structural health monitoring than other conventional methods [ref].

Although PWAS are small, unobtrusive, and inexpensive, the laboratory measurement equipments (e.g., HP4194A impedance analyzer and PC) used in the proof-of-concept demonstration of these technologies are bulky, heavy, and relatively expensive. With few exceptions, most of the research effort to date has been on damage localization and detection methods, largely ignoring the necessity of a compact and low-price hardware system for E/M impedance method in field SHM application.

The development of the compact and low-price hardware system will take place in stages, from PC to laptop, then circuit-board integration, and eventually chip-level integration (Figure 1). The basic concept of the hardware system is such that (1) performs structural health diagnosis with PWAS-based E/M impedance technique; (2) extracts structural health status information by local processing of the signals received by sensors using damage

identification algorithms; (3) transmits wirelessly the diagnostic signals to a monitoring computer via wireless transceiving circuit and also receives signals from the monitoring computer for active sensing and microchip reprogramming purposes.

Figure 1 The road map for the development of an integrated active structural health monitoring system

2. IMPEDANCE MEASUREMENT APPROACHES

In our previous work [2][3], a simplified impedance analyzer system was presented for PWAS E/M impedance measurement (up to 1MHz frequency range). The system utilizes standard low-cost multipurpose laboratory equipments: a function generator, a PCI DAQ card, a PCI GPIB card, a calibrated low value resistor (100Ω) and a PC with LabVIEW software package (Figure 2). By using a PCMCIA interfaced DAQ card and GPIB card, this simplified impedance analyzer can be easily updated to a more compact laptop based version.

Figure 2 Simplified E/M impedance measurement system: (a) hardware configuration; (b) LabVIEW GUI

By using the simplified impedance measurement as a platform, a number of impedance measurement methods were explored. Basically, they can be classified into two categories: (1) measure PWAS impedance spectrum frequency by frequency by using sinusoidal excitation; (2) measure PWAS impedance spectrum by using transfer function approach using broadband excitation.

2.1. Measure PWAS Impedance Spectrum Frequency by Frequency

In order to evaluate the PWAS impedance at certain frequency point, amplitude ratio and phase difference between the input sinusoidal excitation and output sinusoidal response should be measured. Of these two, the phase difference is more difficult to ascertain. Several methods are available for measuring the phase difference between

two sinusoidal signals, including zero crossing, signal integration (the technique used by an HP4194A analyzer), cross-correlation, and Fourier Transform., Among them, the Fourier Transform method shows best performance in terms of measurement speed and accuracy in preliminary testing [2].

Consider a more general sinusoidal waveform for voltage or current with initial phase φ , i.e.,

$$x(t) = A \sin(2\pi ft + \varphi) \quad (1)$$

where, f is the frequency of sine wave, φ is the initial phase of the signal. Performing the DFT of $x(t)$ gives

$$X(k) = A \frac{j}{2} e^{j\varphi} (e^{-j2\pi(q+k)n/N} - e^{-j2\pi(q-k)n/N}), k = 0, 1, 2, \dots, N-1 \quad (2)$$

where, $q = fN/f_s$, N is the number of samples, f_s is the sampling frequency

Note that

$$\begin{cases} X(k) = \frac{A}{2} N \sin \varphi - j \frac{A}{2} N \cos \varphi, k = q, N - q \\ X(k) = 0, \text{otherwise} \end{cases} \quad (3)$$

Eq. (3) allows us to calculate the magnitude, A , and phase, φ , of the signal x .

2.2. Measure PWAS Impedance Spectrum by using transfer function

Alternatively, PWAS impedance spectrum can be measured by using an approach similar to system transfer function identification [3]. For a linear system, by transforming the time domain excitation signal (voltage $[v(t)]$) and response signal (current $[i(t)]$) of the DUT to yield the frequency domain quantities $[V(f)]$ and $[I(f)]$, the admittance, Y , of DUT may be calculated as the transfer function of DUT (see Figure 3)

Figure 3 Configuration for impedance spectrum measurement using transfer function of DUT

Hence, the impedance of DUT is

$$Z(f) = \frac{V(f)}{I(f)} = \frac{FFT\{v(t)\}}{FFT\{i(t)\}} \quad (4)$$

Figure 4 Linear chirp signal (sweep from DC to 1MHz): (a) waveform; (b) amplitude spectrum

To implement this approach, excitation signals with broadband spectrum are need. Two type of digitally synthesized excitation signals have been explored for PWAS impedance measurement: (1) linear chirp signal: Its instant frequency is a linear function of time and its frequency sweeping range and speed can be easily controlled. Figure 4

shows the linear chirp in time domain and frequency domain, respectively; (2) frequency-swept signal. It can be synthesized in frequency domain by defining the magnitude spectrum and group delay of the signal intended to be synthesized. Figure 5 shows a synthesized frequency-swept signal. As compared to the chirp excitation, this type of excitation signal possesses an extremely flat magnitude indicating a uniform SNR and better accuracy for impedance measurement.

Figure 5 Frequency swept signal: (a) waveform; (b) amplitude spectrums

2.3. Comparison of Impedance Measurement Approaches

Both of the impedance measurement approaches, frequency by frequency approach and transfer function approach, presented in the previous sections have their advantages and disadvantages.

For the frequency by frequency approach, it measures impedance spectrum by exciting step by step pure tones of sine waves of increasing frequency. The excitation signal and response signal will both be digitized and computed for amplitude and initial phase information by using Eq. (3) for later complex impedance calculation at each frequency point. The iteration number of the above procedure is equal to the number of the frequency points in the impedance spectrum which is give by the user (the default iteration number is equal to 401 for the HP419A impedance analyzer). In addition to applying Eq. (3), coherent sampling condition has to be satisfied to avoid frequency leakage [4]. Coherent sampling occurs when the following relationship exists:

$$f_s \cdot N_c = f \cdot N \quad (5)$$

where, f_s is the sampling frequency, N_c is the integer number of cycles in the data record, f is the input frequency, N is the number of samples in the data record. To satisfy Eq (5), more considerations need to be taken into account for the system hardware control, such as the sampling frequency selection of ADC and DAC. If the FFT (fast Fourier transform) algorithm is to be used, another requirement appears: the time record should contain 2^n samples, where n is an integer. This shows that the FFT algorithm is not always desirable due to the sample number N constrains. Therefore, DFT instead of FFT is always preferred in the calculation of the iterated procedure. With the increase of iteration number, this method will become time-consuming. More efforts are needed to impellent this approach. However, for this approach using pure sine waves, high SNR is expected at each frequency point. Hence, it provides very high accuracy for PWAS impedance spectrum measurement.

For the transfer function approach, the FFT measures the response at all frequencies within the span simultaneously, thus the excitation must contain energy at all of the measured frequencies. Figure 5 shows that the peak amplitude of excitation is 5V, whereas the amplitude of each frequency component is 0.25V. Since the input range must be set to accommodate the amplitude peak, each frequency component is measure at -26dB relative to full scale. Therefore, a lower SNR ratio and accuracy are expected when using this approach for impedance measurement. However, by utilizing broad-band excitation signals, this approach is able to measure the whole impedance spectrum within one excitation signal sweep. Therefore, it is relatively time-efficient for impedance spectrum measurement.

2.4. Test of Transfer-function-type Impedance Measurement Approach

An aluminum test panel existing in our lab from other experiments [5] was used to test our methods. The panels

consist of the skin (Al 7075, 24x23.5x0.125 in) with a 3 in diameter hole in the center, two spars (Al 6061 I-beams, 3x2.5x0.250 in and 24 in length), four stiffeners (Al 6063, 1x1x0.125 in and 18.5 in length) and fasteners installed from the skin side. The stiffeners were bonded to the aluminum skin using a structural adhesive, Hysol EA 9394. Damages were artificially introduced in the specimen including cracks (CK), corrosions (CR), disbonds (DB), and cracks under bolts (CB).

Figure 6 Schematic of space panel test specimen with crack, corrosion, disbond damages

In this experiment, we tested the detection of DB1 (disbond #1, size: 2x0.5 in) by measuring E/M impedance of PWAS a1, PWAS a2, and PWAS a3, we used the simplified E/M impedance analyzer system (using frequency-swept excitation with 256-time average) in parallel with the traditional HP4194A impedance analyzer, and compared the results.

Figure 7 Real part impedance spectrums of PWAS a1, PWAS a2, a3 with 256-time average: (a) measured by simplified E/M impedance analyzer using frequency-swept excitation; (b) measured by HP4194A impedance analyzer

The real part impedance spectrums from PWAS a1, PWAS a2, and PWAS a3 are presented in Figure 7. It can be seen that the impedance spectrums from PWAS a1 and PWAS a3 located on the area with good bond are almost identical. The spectrum from PWAS a2 located on the disbond DB1 is very different showing new strong resonant peaks associated with the presence of the disbond. Both the simplified impedance analyzer and HP4194 impedance analyzer can detect the presence of DB1 disbond on the test panel. The peaks in impedance spectrums from simplified analyzer and HP4194A impedance analyzer are in good agreement. Although, as presented in section 2.3, broad-band excitation offers lower accuracy for PWAS impedance measurement than pure-tone sinusoidal excitation, it provides a good compromise between the accuracy and time-efficient for E/M impedance measurement

for structural health monitoring.

3. DSP-BASED IMPEDANCE ANALYZER

As indicated in our road map (Figure 1), the next development stage of the compact impedance analyzer will be the circuit-board integration which eliminates PC/laptop control in the simplified impedance analyzer system. All the explored impedance measurement approaches will be implemented and tested on this new platform. The system will be able to measure E/M impedance at least up to 1MHz.

3.1. System Hardware Configuration

Figure 8 shows the development platform of the DSP-based impedance analyzer system. It consists of a TI C6416T DSK board operating at 1GHz and functioning as the computation core of the system, a Signalware AED101 analog expansion daughter card providing 2-channel ADCs and DACs with sampling rate up to 80MHz, a 50kHz~1.5MHz band-pass smoothing filter for eliminating spurious frequency components in DAC output, and a PC power source (+5V, +12V, -12V).

Figure 8 Hardware configuration of the DSP-based impedance analyzer system

Figure 9 Block diagram of C6416T DSK board

The DSP on the 6416T DSK interfaces to on-board peripherals through one of the two busses, the 64-bit wide EMIFA and the 8-bit wide EMIFB (Figure 9). EMIFA is connected to daughter card expansion connectors providing communications between DSP and the analog expansion daughter card [6].

Figure 9 shows the block diagram of the Signalware AED101 analog expansion daughter card [7]. The AED101 has a wide variety of applications that require high sample rates for one or two channels input/output. The inputs can be sampled at 12bits, 80MS/s with the ADS809Y A/D converter. The two THS5661A D/A converters support an output of 12bits up to 80MS/s. The advantages of this daughterboard over boards that contain only the A/D and D/A converter is that it provides breadboard space for analog signal conditioning circuits and a Field Programmable Gate Array (Xilinx Virtex XCV50E FPGA) for digital preprocessing before the sampled data is placed in the DSP memory. This allows prototypes with the complete front end design which is often essential to successful development in high performance applications of the DSP. The inputs to the A/D converter and the output from the D/A converters can connect directly to a breadboard area on which conditioning circuits can be constructed. The A/D and D/A converters have their parallel digital interface connected directly to the Xilinx FPGA which provides a flexible digital interface to the DSP. Table 1 lists all the available FPGA registers which are memory-mapped and provide the ability to operate the ADCs and DACs sampling rate, ADC FIFO and DCA FIFO, DSP external interrupt generation, digital I/O, etc.

Figure 10 Block diagram of Signalware AED101 analog expansion daughter card

Table 1 Daughter card FPGA registers

Register name	Register category & function
•A/D and D/A Status	} A/D FIFO overflow & D/A FIFO underflow registers
•Interrupt Start	
•Interrupt Period	} EXT_INT4 interrupt generation control registers
•Interrupt Down Counter	
•A/D Clock Rate	} ADC registers
•A/D Clock Down Counter	
•A/D FIFO (512 words)	
•D/A Clock Rate	} DAC registers
•D/A Clock Down Counter	
•D/A FIFO (512 words)	
•Digital I/O	} Digital I/O registers
•Digital I/O control	

A band-pass filter was designed with TI filter Pro software and built on a separate PCB board to smooth the excitation signal generated by DAC. The band-pass (50kHz~1.5MHz) filter was constructed by connecting a Sallen-key 4-pole high-pass Butherworth filter with a Sallen-key 4-pole low-pass Butherworth filter. Figure 11 shows the frequency response and circuit of the band-pass filter.

Figure 11 Frequency response and circuit of the band-pass smoothing filter: (a) high-pass filter with 50kHz cut-off frequency; (b) low-pass filter with 1.5MHz cut-off frequency.

3.2. System State Diagram for System Excitation Signal Generation and Data Acquisition

The DSP-base impedance analyzer system can be mainly divided into four functional modules: signal source generation, data acquisition, impedance evaluation and damage evaluation. Impedance evaluation methods have been discussed in section 2. As for damage evaluation module, it may vary in different applications and will not be covered in this paper. In this section, implementation of signal source generation and data acquisition on the DSP platform will be presented.

To digitize voltage and current (also in terms of voltage) for later impedance measurement, two ADCs are needed in the system. In addition, a DAC with smoothing filter is needed to generate the excitation signals. The ADCs and DAC will be started simultaneously by setting FPGA start signal (CNTL0 from DSK) and synchronized by an EMIF clock signal from DSK. In this synchronous mode, A word will be read into ADC FIFO and write to DAC from DAC FIFO at each rising edge of the EMIF clock signal. Both of the ADC FIFO and DAC FIFO are 512-word FIFO. When the DSP reads from the ADC data address, one word is read from the ADC FIFO. If a read is performed when FIFO is empty an ADC FIFO underflow will occur. When the DSP writes to the DAC data address, one word is written into the DAC FIFO. If a write is performed when the FIFO full, a DAC FIFO overflow will occur. To avoid the underflow and overflow, a count-down counter configured in the FPGA and clocked by the same EMIF clock will be used to count the word numbers in the ADC FIFO and DAC FIFO. Every time the counter counts from a pre-determined value to zero, a pulse is sent to EXT_INT4 pin of the DSP. If the DSP external interrupt #4 is enabled, an interrupt subroutine will be called. In the interrupt subroutine, operations, such as read ADC FIFO and refill DAC FIFO via EDMA (enhanced direct memory access), can be preformed.

To run the system, the CNTL0 line must be made high. At that time, both the ADC and DAC will begin to transfer data. Some DAC data should be written to the DAC FIFO before asserting CNTL0, otherwise the DAC FIFO will immediately underflow.

Figure 12 shows the state diagram for operating ADC and DAC in synchronous mode without underflow and overflow. State1 performed all needed initializations. It writes to DAC FIFO 512 words to avoid DAC underflow, prepares all needed reload/link ParaRams, setups EXT_INT4 as EDMA channel 4 trigger event, and setups EDMA channel 8 chained to channel 4. Thus, EDMA channel 4 is trigger by EXT_INT4 event; channel 8 will be activated for data transmission after the completion of channel 4 data transmission; and channel 4 and channel 8 EDMA parameters will be updated by their link setups. Also, state1 sets counter initial value equal to 256. Therefore, every 256 EMIF clock signals, an EXT_INT4 interrupt signal will be generated; 256 words data in ADC FIFO will be

read via EDMA channel 4; DAC FIFO will be refilled via EDMA channel 8. In the state diagram, CIPR[4] and CIPR[8] denote the transmission completion of EDMA channel 4 and EDMA channel 8, respectively. After transmission completion of EDMA channel 4, which read in 256 words from ADC FIFO on each EDMA event, CIPR[4] gets set. When CIPR[4] gets set, EDMA channel 4 will update its destination address setup in state4. At the same time, CIPR[4] set will trigger EDMA channel 8 to initiate a writing of 256 words to DAC FIFO. After the transmission completion of EDMA channel 8, CIPR[8] gets set and the program goes to state6 where EDMA channel 8 updates its source address. Thus, provided appropriate sampling rate for ADC and DAC, the system will loop until wanted length of data is recorded and never get underflow or overflow problems [7][8].

Figure 12 System excitation signal generation and data acquisition state diagram

Figure 13 ADC sampled 100kHz sine waves with 768 data points (sampling rate: 8MHz)

Figure 14 100kHz sine wave output by DAC with 4MHz sampling rate

Preliminary tests for ADC data acquisition and DAC excitation signal generation have been performed by using the state diagram in Figure 12. Figure 13 and Figure 14 show the recorded two sine waves and generated excitation sine wave, respectively. As shown in Figure 13, the recorded data length is equal to 768 three times of 256. The EDMA channel 4 link number is set equal to 3 to read back 768 points sine waves continuously (more data points, i.e., larger link number may be needed for impedance measurement). Figure 14 shows the 100kHz sine wave generated by ADC converter before smoothing filter and after smoothing filter. As we can see, smoothing filter improved the ADC output to some extent.

4. DISCUSSIONS AND FURTHER WORK

The development of a compact and low-cost impedance analyzer system was presented in this paper. In the first part, two types of impedance measurement approaches were explored. One approach measures impedance frequency by frequency offering very high accuracy. However, this approach is not time-efficient and needs more efforts to be implemented. The other approach measures impedance by using broad-band excitation and transfer function method providing a good compromise among the measurement time-efficient, accuracy and implementation efforts. Experimental results show that the latter approach can be used for E/M impedance method for structural health monitoring. In the second part, a DSP-based impedance analyzer system was studied. The system consists of a PC power source, a TI C6416 DSK, and an analog expansion daughter card. The daughter card has breadboard space for analog signal conditioning circuits and a FPGA providing digital interfaces to ADCs and DACs. This offers an easy modification and control of the system hardware. To operate ADC and DAC in synchronous mode for impedance measurement, the system software state diagram was presented in details. Preliminary testing of the system shows that the system is a good candidate for building compact impedance analyzer system for SHM. More work needs to be done for implementing the explored impedance measurement approaches in the system in the future.

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REFERENCES

1. Park, G.; Sohn, H.; Farrar, C. R.; Inman, D. J. (2003) "Overview of Piezoelectric Impedance-Based Health

Monitoring and Path Forward”, *The Shock and Vibration Digest*, Vol. 35, pp. 451-463, 2003

2. Giurgiutiu, V.; Xu, B. (2004) “Development of a Field-Portable Small-Size Impedance Analyzer for Structural Health Monitoring using the Electromechanical Impedance Technique”, *SPIE's 11th Annual International Symposium on Smart Structures and Materials and 9th Annual International Symposium on NDE for Health Monitoring and Diagnostics*, 14-18 March 2004, San Diego, CA. paper # 5391-923
3. Giurgiutiu, V.; Xu, B. (2005), “ Efficient Electromechanical (E/M) Impedance Measuring Method for Active Sensor Structural Health Monitoring”, *SPIE's 12th International Symposium on Smart Structures and Materials and 10th International Symposium on NDE for Health Monitoring and Diagnostics, Sensors and Smart Structures Technologies for Civil, Mechanical, and Aerospace Systems*, San Diego, CA, 7-10 March, 2005, paper # 5765-30
4. IEEE Std 1057-1994 (2001), IEEE standard for digitizing waveform recorders, 2001 Revision
5. Cuc, A.; Tidwell, Z.; Giurgiutiu, V.; et al (2005), “Non-Destructive Evaluation (NDE) of Space Application Panels Using Piezoelectric Wafer Active Sensors”, *2005 ASME International Mechanical Engineering Congress and Exposition*, Orlando, FL, 5-11 Nov., 2005, paper # IMECE2005-81721
6. TI (2004), “ TMS320C6416T DSK Technical Referece”, 508035-001 Rev A, Nov, 2004
7. Signalware (2004), “AED-101 wide bandwidth Analog Expansion Daughter Board”, Rev 1.2, April, 2004
8. Kehtarnavaz, N. (2004), *Real-time Digital Signal Processing Based on the TMS320C6000*, Newnes, 2004